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RM-6525

B. E. II (Sem. IV) (IC) Examination

May / June – 2010

Pulse & Switching Circuit

Time : **3** Hours] [Total Marks : **100**

Instruction :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. 2 (Sem. 4) (IC)**

Name of the Subject :

☛ **Pulse & Switching Circuit**

☛Subject Code No. : **6 5 2 5** ☛Section No. (1, 2,.....) : **1&2**

Seat No. :

Student's Signature

(2) Attempt all questions.
(3) Figures to the **right** indicate full marks.
(4) Assume suitable data wherever **necessary**.
(5) Answers to the **two** sections must be written in **separate** answer books.

1 (a) Answer the following : **10**

(i) The waveform which preserves its form when transmitted through linear network is _____.

(ii) Diode clippers are used only for one level clipping _____. (True/False)

(iii) The lower cut-off frequency of a low pass circuit is _____.

(iv) A high pass circuit acts as a _____ if the time constant of the circuit is very small in comparison with the time required for the input signal to make an appreciable change.

(v) Clipping circuits require non-linear elements _____ (True/False)

(vi) Clipping circuits are _____ comparators.

(vii) The _____ circuit is often referred to as dc restorer.

(viii) Energy storage elements are must for clipping circuits _____ (True/False)

(ix) In _____ clamping the negative extremity of the waveform is fixed at the reference level and the entire waveform appears above the reference.

(x) A signal which maintains the value zero for all times $t < 0$ and maintains the value V for all times $t \geq 0$ is called a _____.

(b) With the help of a neat circuit diagram explain the working of a two-level diode clipper. **6**

(c) Explain the clamping theorem. **4**

2 (a) A 10 Hz symmetrical square wave whose peak to peak amplitude is 2V is impressed upon a high-pass RC circuit whose lower 3 dB frequency is 5 Hz. Calculate and sketch the output waveform for the first two cycles. What is the peak-to-peak output amplitude under steady-state conditions? **10**

(b) Draw the transfer characteristics for the circuit shown in figure 1. Also draw the output waveform for a sinusoidal input of amplitude 20 V peak. **5**

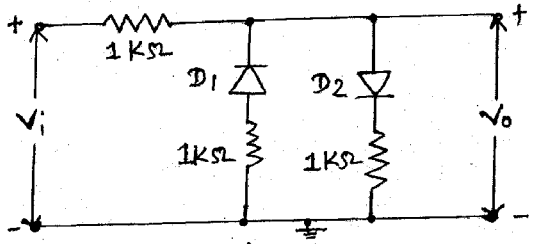

fig. 1.

OR

2 (a) In the clamping circuit shown in figure 2 R_s = R_f = 50 Ω, R = 20 k Ω and C = 2 Ω. A symmetrical square wave signal of amplitude 20 V and frequency 5 kHz is applied at t=0. Draw the first three cycles of the output waveform. **10**

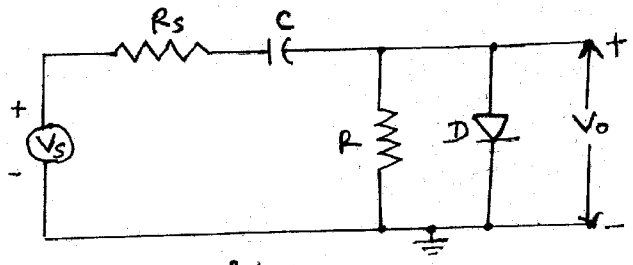

fig. 2

(b) For sinewave input to the clipper circuit shown in figure 3 and figure 4, plot output voltage waveform. **5**

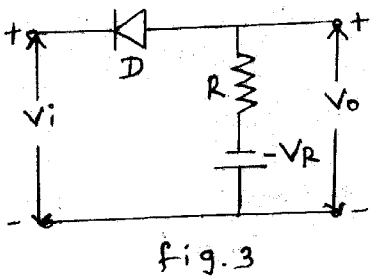

fig. 3

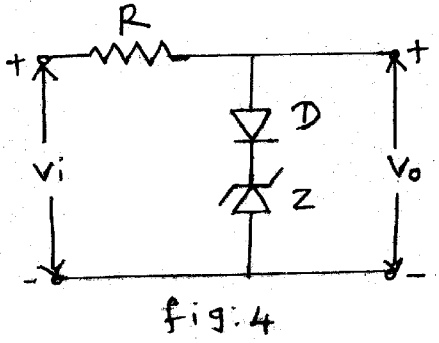

fig. 4

3 (a) Compute and draw to scale the outut waveform for (a) C_1 = 50 PF, (b) C_1 = 75 pF and (c) C1 = 25 pF respectively for the circuit shown in figure 5. The input is a 20 V step. 8

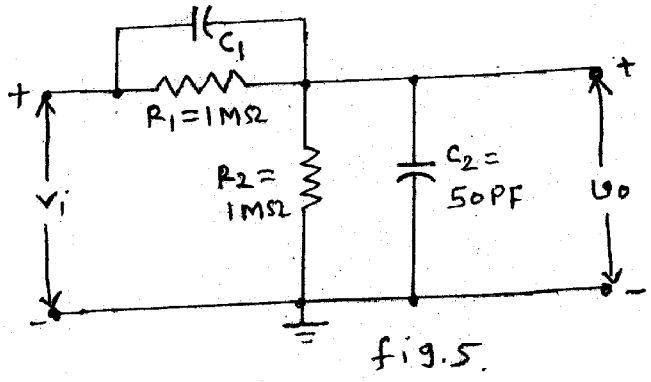

fig.5.

(b) Derive the expression for the percentage tilt for the square input, which is applied to high pass RC circuit. 7

OR

3 (a) Assuming that the capacitor is initially uncharged, determine the output response of the low-pass RC circuit with time constant 0.05 mS, to the input waveform shown in figure 6. 10

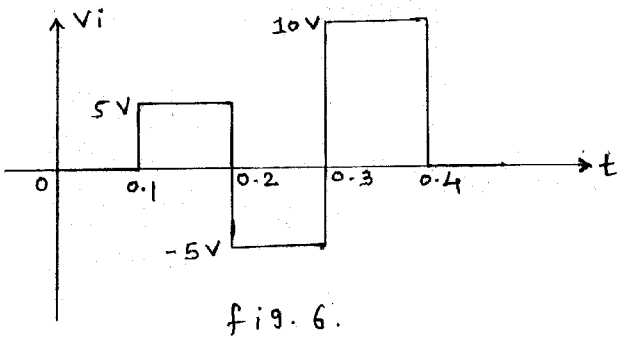

fig. 6.

(b) Design a diode clamper to restore a dc level of +5V to an input signal of peak to peak value of 20 V. 5

SECTION - II

4 (a) Attempt the following : 10

(i) During transition, the loop gain is _____.

(ii) The _____ multivibrator is used as a master oscillator.

(iii) _____ triggering is used in binary counting circuits.

(iv) Two or more generators are said to be running _____ if all of them arrive at some reference point in the cycle at exactly the same instant of time.

(v) When generators with equal frequencies run in synchronism, the synchronization is said to be on a _____.

(vi) Counting circuits are an examples of synchronization with _____.

(vii) The reciprocal of the resolving time of the flip-flop is the _____ at which the binary will respond.

(viii) What is the use of collector catching diodes?

(ix) Define blocked condition.

(x) Define resolving time.

(b) Explain non saturating binary. **5**

(c) Explain triggering symmetrically through a unlaterial device **5**

5 (a) For a circuit diagram shown in figure 7 $V_{CC} = V_{BB} = 6$ V, $R_c = 1.2$ kΩ, $R_1 = 4.7$ kΩ, $R_2 = 27$ KΩ. Find h_{FE}(min) and stable state voltages and currents. Take V_{CE}(sat) = 0.5 V, V_{BE}(sat) = 1V.

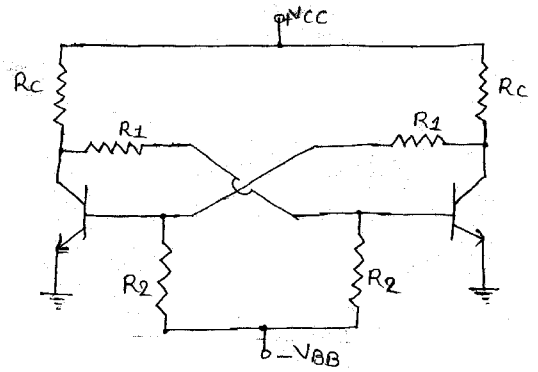

Fig. 7

(b) Write a short note on DCTL. **5**

OR

5 (a) Derive the expression of gate width T of a monostable multivibrator by neglecting the reverse saturation current I_{CBO}. **5**

(b) Silicon transistors with h_{FE}(min) equal to 20 are available. If $V_{CC}=V_{BB} = 10$ V, design the bistable multivibrator. **10**

6 (a) Design a Schmitt trigger circuit to have $V_{CC} = 12$ V, $U_{TP} = 6$V, $L_{TP} = 3$V, using two silicon n-p-n transistors with h_{FE}(min) = 60. Take $I_{C2} = 2$mA and $V_{r1}=0.5$ V. **8**

(b) Draw and explain collector coupled monstable multivibrator. **7**

OR

6 (a) Silicon n-p-n transistor with h_{FE}(min) = 40 are available. Design an astable multivibrator to generate a square wave 1 kHz frequency with a duty cycle of 25%. **8**

(b) Explain the working of Emitter coupled astable multivibrator with the help of circuit diagram and waveform. **7**